

**SEMICONDUCTOR DEVICE AND
METHOD FOR FABRICATING THE SAME**

BACKGROUND OF THE INVENTION

5 The present invention relates to a semiconductor device, including metal interconnects laid in an insulating film with a low dielectric constant (which will be herein called a low-dielectric-constant film), and also relates to a method for fabricating the same.

10 Hereinafter, the structure of a semiconductor device, including inlaid metal interconnects in a low-dielectric-constant film, will be described with reference to FIG. 6.

As shown in FIG. 6, a second insulating film 102 is formed of a silicon dioxide film, for example, on a first insulating film 101 deposited on a semiconductor substrate 100.
15 In the second insulating film 102, metal interconnects 105 have been formed. Specifically, each of the metal interconnects 105 consists of a barrier metal layer 105a of tantalum nitride, for example, and a main interconnect layer 105b of
20 copper, for instance.

In this semiconductor device, the second insulting film 102, which exists between the metal interconnects 105, is made of silicon dioxide with a dielectric constant between about 3.9 and about 4.2. Therefore, a parasitic capacitance,
25 generated between the metal interconnects 105, increases,

thereby interfering with high-speed operation of the semiconductor device.

To solve this problem, a carbon-containing silicon dioxide film with a low dielectric constant of about 2.5 may be
5 used as the second insulating film 102.

Hereinafter, a method for fabricating a semiconductor device, including inlaid metal interconnects formed in an insulating film of carbon-containing silicon dioxide, will be described with reference to FIGS. 7A through FIGS. 7E.

10 First, as shown in FIG. 7A, a second insulating film 110 of carbon-containing silicon dioxide, is deposited on a first insulating film 101 formed on a semiconductor substrate 100. Then, a resist pattern 111 with openings for forming interconnect grooves is defined on the second insulating film 110
15 as shown in FIG. 7B.

Next, as shown in FIG. 7C, the second insulating film 110 is plasma-etched using an etching gas, consisting essentially of fluorine and carbon, and being masked with the resist pattern 111. In this manner, interconnect grooves 112
20 are formed in the second insulating film 110. As a result, the upper part of the resist pattern 111 changes into a cured layer 111a. Specifically, the bonding states of atoms in the cured layer 111a are different from those of atoms in the original material of the resist pattern 111 that has not yet
25 been plasma-etched. And the cured layer 111a is made of a

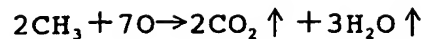
polymer consisting essentially of fluorine and carbon and has a thickness of about 50 nm. The cured layer 111a cannot be removed by a wet etching process but can be removed by a plasma etching process using oxygen gas.

5 Accordingly, the resist pattern 111 is ashed away with oxygen plasma as shown in FIG. 7D. In this case, the ashing process is performed by a down flow technique (in which no bias voltage is applied to the substrate) in a vacuum between about 267Pa and about 400Pa, for example, and with the sub-
10 strate heated to a relatively high temperature between about 150°C and about 250°C, for instance. In this manner, the resist pattern 111 with the cured layer 111a in its upper part can be stripped just as intended. Also, a silicon dioxide film 113 with a thickness of 200 nm, for example, is formed
15 in the upper part of the second insulating film 110 of carbon-containing silicon dioxide.

 In the ashing process using oxygen plasma, carbon is removed from the carbon-containing silicon dioxide for the second insulating film 110, thereby producing silicon dioxide.
20 Hereinafter, this mechanism will be described with reference to FIGS. 8 and 9.

 FIG. 8 illustrates an example of a chemical formula representing a carbon-containing silicon dioxide. If the carbon-containing silicon dioxide represented by this chemical for-
25 mula and oxygen are bonded together, the following chemical

reaction



occurs. Then, CH_3 , which has been bonded to Si, disappears. That CH_3 disappeared is replaced with O to form SiO_2 bonds.

5 Therefore, a silicon dioxide as represented by the chemical formula shown in FIG. 9 is produced.

Next, a tantalum nitride film is deposited over the second insulating film 110, or on the silicon dioxide film 113 more exactly, by a sputtering process. And then, a copper
10 film is deposited on the tantalum nitride film by an electroplating process. Thereafter, excessive parts of the copper and tantalum nitride films, existing over the second insulating film 110, are removed by a CMP process, thereby defining metal interconnects 114 as shown in FIG. 7E. The metal inter-
15 connects 114 are made up of a barrier metal layer 114a of tantalum nitride and a main interconnect layer 114b of copper.

However, the semiconductor device formed in this manner has the following problems.

20 First of all, in the step of ashing away the resist pattern 111 using oxygen plasma, the silicon dioxide film 113 is adversely formed in the upper part of the second insulating film 110 of carbon-containing silicon dioxide. Specifically, the silicon dioxide film 113 exhibits a high dielectric con-
25 stant and has a thickness of 200 nm, for example. Therefore,

although the carbon-containing silicon dioxide film is used as the second insulating film 110, a parasitic capacitance generated between the metal interconnects 114 cannot be reduced sufficiently.

5 Also, the silicon dioxide film 113 has a density between 1.7 g/cm³ and 1.8 g/cm³, which is lower than that of a silicon dioxide film formed by a plasma CVD process, for instance. Therefore, when oxygen plasma is supplied in a subsequent process step, oxygen ions go through the silicon dioxide film 10 113 to reach and oxidize the carbon-containing silicon dioxide film under the film 113. As a result, the silicon dioxide film 113 has its film thickness increased undesirably. This phenomenon is observed, for example, in the subsequent process step of ashing away a resist pattern for forming via 15 holes over the metal interconnects 114. The phenomenon is also observed, for instance, in the subsequent process step of ashing away a resist pattern for forming interconnect grooves for upper-level metal interconnects to be formed over the via holes.

20 As described above, in the known semiconductor device including inlaid metal interconnects in an insulating film of carbon-containing silicon dioxide, a thick silicon dioxide film is unintentionally formed in upper parts of the insulting film that surround the metal interconnects. As a result, 25 a parasitic capacitance generated between the metal intercon-

nects increases disadvantageously.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to
5 enhance the performance of a semiconductor device, including
inlaid metal interconnects in an insulating film of carbon-
containing silicon dioxide, by reducing a parasitic capaci-
tance produced between the metal interconnects.

To achieve this object, a first inventive semiconductor
10 device includes: an insulating film formed of a carbon-
containing silicon dioxide film on a substrate; an intercon-
nect groove formed in the insulating film; a silicon dioxide
layer, which is formed on the bottom and side faces of the
interconnect groove and has a density high enough to allow
15 almost no oxygen to pass therethrough; and a metal intercon-
nect formed on the silicon dioxide layer inside the intercon-
nect groove.

In the first inventive device, the silicon dioxide layer
with a density high enough to allow almost no oxygen to pass
20 therethrough is formed on the bottom and side faces of the
interconnect groove. Therefore, even if oxygen plasma is sup-
plied in a subsequent process step, oxygen ions cannot pass
through the silicon dioxide layer, and the carbon-containing
silicon dioxide film surrounding the silicon dioxide layer is
25 not oxidized. Accordingly, the thickness of the silicon diox-

ide layer, existing on the bottom and side faces of the interconnect groove, does not increase. As a result, a parasitic capacitance produced between the metal interconnects can be reduced just as intended.

5 In one embodiment of the first device, the silicon dioxide layer preferably has a density of 2.0 g/cm^3 or more.

In such an embodiment, the silicon dioxide layer prevents the oxygen ions from passing therethrough with much more certainty. As a result, it is possible to suppress the
10 increase in thickness of the silicon dioxide layer existing on the bottom and side faces of the interconnect groove.

A second inventive semiconductor device includes: an insulating film formed of a carbon-containing silicon dioxide film on a substrate; an interconnect groove formed in the insulating film; a silicon dioxide layer, which is formed on
15 the bottom and side faces of the interconnect groove and has a small and uniform thickness; and a metal interconnect formed on the silicon dioxide layer inside the interconnect groove.

20 In the second inventive device, the silicon dioxide layer with a small and uniform thickness is formed on the bottom and side faces of the interconnect groove. In other words, the silicon dioxide layer, existing between the metal interconnects, has a high dielectric constant and a small and
25 uniform thickness. As a result, a parasitic capacitance pro-

duced between the metal interconnects can be reduced just as intended.

In one embodiment of the second device, the silicon dioxide layer preferably has a thickness of 20 nm or less.

5 In such an embodiment, the parasitic capacitance produced between the metal interconnects can be further reduced.

A first inventive method for fabricating a semiconductor device includes the steps of: a) forming an insulating film of a carbon-containing silicon dioxide film on a substrate; 10 b) etching the insulating film using a resist pattern as a mask, thereby forming an interconnect groove in the insulating film; c) performing a dry etching process using an etching gas containing oxygen, thereby removing a cured layer and forming a silicon dioxide layer on the bottom and side faces 15 of the interconnect groove; d) removing the resist pattern by a wet etching process; and e) filling the interconnect groove with a metal film to form a metal interconnect. The cured layer has been formed in an upper part of the resist pattern as a result of the step b).

20 According to the first inventive method, by performing a dry etching process using an etching gas containing oxygen, a cured layer, formed in an upper part of a resist pattern as a result of the step b), is removed and a silicon dioxide layer is formed on the bottom and side faces of an interconnect 25 groove. Therefore, the bottom and side faces of the intercon-

nect groove are exposed to the etching gas containing oxygen for just a short time. Accordingly, a silicon dioxide layer with a small and uniform thickness is formed on the bottom and side faces of the interconnect groove. Also, the resist pattern having the cured layer removed is stripped by a wet etching process. Therefore, in the step d), the bottom and side faces of the interconnect groove are not exposed to the oxygen plasma, and the thickness of the silicon dioxide layer does not increase. Consequently, it is possible to reduce a parasitic capacitance produced between the metal interconnects just as intended.

In one embodiment of the first method, the dry etching process is preferably performed within a plasma ambient at a pressure of 13.3 Pa or less.

Then, a silicon dioxide layer with a thickness of about 20 nm or less can be formed on the bottom and side faces of the interconnect groove. As a result, the parasitic capacitance produced between the metal interconnects can be further reduced.

In this particular embodiment, the dry etching process is preferably an anisotropic RIE process.

In such an embodiment, a silicon dioxide layer with a thickness of about 20 nm or less and a density high enough to allow almost no oxygen to pass therethrough can be formed on the bottom and side faces of the interconnect groove. There-

fore, even if oxygen plasma is supplied in a subsequent process step, oxygen ions cannot pass through the silicon dioxide layer, and a carbon-containing silicon dioxide film surrounding the silicon dioxide layer is not oxidized. Accordingly,
5 the thickness of the silicon dioxide layer, existing on the bottom and side faces of the interconnect groove, does not increase. As a result, the parasitic capacitance produced between the metal interconnects can be reduced just as intended.

10 In another embodiment, the first inventive method preferably further includes the step of removing the silicon dioxide layer, existing on the bottom and side faces of the interconnect groove, by a wet etching process.

In such an embodiment, the silicon dioxide layer with a
15 high dielectric constant no longer exists between the metal interconnects. As a result, the parasitic capacitance produced between the metal interconnects can be further reduced.

A second inventive method for fabricating a semiconductor device includes the steps of: a) forming an insulating
20 film of a carbon-containing silicon dioxide film on a substrate; b) etching the insulating film using a resist pattern as a mask, thereby forming an interconnect groove in the insulating film; c) filling the interconnect groove with a resist film; d) removing a part of the resist film, existing
25 over the interconnect groove, and the resist pattern with a

cured layer by a dry etching process using an etching gas containing oxygen; e) removing the other part of the resist film, still existing inside the interconnect groove, by a wet etching process; and f) filling the interconnect groove with
5 a metal film to form a metal interconnect. The cured layer has been formed in an upper part of the resist pattern as a result of the step b).

In the second inventive method, an interconnect groove is filled with a resist film and then a cured layer, existing
10 in an upper part of a resist pattern, is removed by a dry etching process using an etching gas containing oxygen. Therefore, the bottom and side faces of the interconnect groove are not exposed to the etching gas containing oxygen, and no silicon dioxide layer is formed thereon. The other
15 part of the resist film, still existing in the interconnect groove, is removed by a wet etching process. Accordingly, the bottom and side faces of the interconnect groove are not exposed to the oxygen plasma, and no silicon dioxide layer is formed thereon in the step e). As a result, a parasitic ca-
20 pacitance produced between the metal interconnects can be reduced just as intended.

In one embodiment, the second inventive method preferably further includes the step of performing an anisotropic RIE process between the steps e) and f) within a plasma ambi-
25 ent containing oxygen at a pressure of 13.3 Pa or less to

form a silicon dioxide layer on the bottom and side faces of the interconnect groove.

In such an embodiment, it is possible to form a silicon dioxide layer with a thickness of about 20 nm or less and a density high enough to allow almost no oxygen to pass there-
through on the bottom and side faces of the interconnect groove. Therefore, even if oxygen plasma is supplied in a subsequent process step, oxygen ions cannot pass through the silicon dioxide layer, and a carbon-containing silicon dioxide film surrounding the silicon dioxide layer is not oxidized. As a result, the parasitic capacitance produced between the metal interconnects can be reduced just as intended.

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BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional view of a semiconductor device according to a first embodiment of the present invention.

FIGS. 2A through 2F are cross-sectional views illustrating respective process steps for fabricating a semiconductor device according to a second embodiment of the present invention.

FIGS. 3A through 3F are cross-sectional views illustrating respective process steps for fabricating a semiconductor device according to a third embodiment of the present inven-

tion.

FIGS. 4A through 4G are cross-sectional views illustrating respective process steps for fabricating a semiconductor device according to a fourth embodiment of the present invention.

FIGS. 5A through 5D are cross-sectional views illustrating respective process steps for fabricating a semiconductor device according to a modified example of the fourth embodiment.

FIG. 6 is a cross-sectional view of a known semiconductor device.

FIGS. 7A through 7E are cross-sectional views illustrating respective process steps for fabricating another known semiconductor device.

FIG. 8 illustrates an example of a chemical formula representing a carbon-containing silicon dioxide.

FIG. 9 illustrates a chemical formula representing a silicon dioxide obtained when oxygen and a carbon-containing silicon dioxide are bonded together.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

EMBODIMENT 1

Hereinafter, a semiconductor device according to a first embodiment of the present invention will be described with reference to FIG. 1.

FIG. 1 illustrates a cross-sectional structure of the semiconductor device according to the first embodiment. A first insulating film 2 of silicon dioxide is formed on a silicon substrate 1. And a second insulating film 3 of carbon-containing silicon dioxide is deposited to a thickness of 1000 nm on the first insulating film 2 by a plasma CVD process or an SGO process, for example.

In the second insulating film 3, interconnect grooves 5 are formed. And a silicon dioxide layer 6 is formed on the bottom and side faces of the interconnect grooves 5. The silicon dioxide layer 6 has a uniform thickness of about 20 nm or less, preferably between about 10 nm and about 15 nm, and a high density between about 2.0 g/cm³ and about 2.1 g/cm³.

On the silicon dioxide layer 6 inside the interconnect grooves 5, metal interconnects 7 are formed. Each of the interconnects 7 is made up of a barrier metal layer 7a of tantalum nitride and a main interconnect layer 7b of copper.

In the semiconductor device of the first embodiment, the silicon dioxide layer 6 with a uniform thickness of about 20 nm or less is formed on the bottom and side faces of the interconnect grooves 5. Therefore, a parasitic capacitance generated between the metal interconnects 7 is reduced significantly. Further, the silicon dioxide layer 6 can improve the adhesiveness of the second insulating film 3 of

carbon-containing silicon dioxide to the metal interconnects 7. As a result, the adhesiveness of the interconnects 7 to the grooves 5 increases.

Furthermore, the silicon dioxide layer 6 with a high density between about 2.0 g/cm^3 and about 2.1 g/cm^3 is formed on the bottom and side faces of the interconnect grooves 5, thus allowing almost no oxygen to pass therethrough. Therefore, even if oxygen plasma is supplied in a subsequent process step, oxygen ions cannot pass through the silicon dioxide layer 6. Accordingly, the carbon-containing silicon dioxide film surrounding the silicon dioxide layer 6 is not oxidized, and the thickness of the silicon dioxide layer 6, formed on the bottom and side faces of the interconnect grooves 5, does not increase. As a result, the parasitic capacitance generated between the metal interconnects 7 can be reduced just as intended. This phenomenon is observed, for example, in the subsequent process step of ashing away a resist pattern for forming via holes over the metal interconnects 7. The phenomenon is also observed, for instance, in the subsequent process step of ashing away a resist pattern for forming interconnect grooves for upper-level metal interconnects to be formed over the via holes.

EMBODIMENT 2

Hereinafter, a method for fabricating a semiconductor

device according to a second embodiment of the present invention will be described with reference to FIGS. 2A through FIGS. 2F.

First, as shown in FIG. 2A, a first insulating film 12 of silicon dioxide is formed on a silicon substrate 11. And a second insulating film 13 is deposited on the first insulating film 12. The second insulating film 13 is formed of a carbon-containing silicon dioxide film with a thickness of 1000 nm by a plasma CVD process or an SOG process, for example.

Next, the second insulating film 13 is coated with a resist film. Subsequently, the resist film is exposed to KrF excimer laser and patterned. Then, the patterned resist film is developed, thereby defining a resist pattern 14 with openings for forming interconnect grooves on the second insulating film 13 as shown in FIG. 2B.

Subsequently, the second insulating film 13 is dry-etched with a plasma, thereby forming interconnect grooves 15 with a depth of about 500 nm in the second insulating film 13 as shown in FIG. 2C. Specifically, the plasma is created from an etching gas obtained by adding argon or oxygen gas to an etching gas consisting essentially of fluorine and carbon (e.g., gas containing at least one of CF_4 and CHF_3 gases). In this manner, the upper part of the resist pattern 14 changes into a cured layer 14a. Specifically, the bonding states of

atoms in the cured layer 14a are different from those of atoms in the original material of the resist pattern 14, which has not yet been plasma-etched. And the cured layer 14a is made of a polymer consisting essentially of fluorine and carbon and has a thickness of about 50 nm.

Next, as shown in FIG. 2D, the cured layer 14a is removed by a plasma etching process with oxygen gas. In this process step, the resist pattern 14 under the cured layer 14a is also removed slightly, but this will not cause a serious problem. Also, in this process step, the surface of the interconnect grooves 15 in the second insulating film 13 are also exposed to the oxygen plasma, thus forming a silicon dioxide layer 16 on the bottom and side faces of the interconnect grooves 15. However, the plasma etching process is performed using the oxygen gas just to remove the cured layer 14a only. Therefore, it takes a much shorter time to perform this plasma etching process than the plasma etching process for removing the resist pattern 14 entirely. Thus, oxygen ions in the plasma cannot go deeper into the second insulating film 13 of carbon-containing silicon dioxide through its surface. As a result, the thin silicon dioxide layer 16 is formed on the bottom and side faces of the interconnect grooves 15.

Hereinafter, it will be described what are the conditions of the plasma etching process using the oxygen gas.

In a first etching method, an etching process is performed for a short time by a down flow technique in a vacuum of 13.3 Pa or less so that the cured layer 14a is removed with most of the resist pattern 14 left. According to this method, oxygen ions in the plasma cannot go deeper into the second insulating film 13 of carbon-containing silicon dioxide through its surface. As a result, a silicon dioxide layer 16 with a thickness of about 20 nm or less is formed on the bottom and side faces of the interconnect grooves 15.

In a second etching method, an anisotropic RIE (reactive ion etching) process, in which a bias voltage is applied to the silicon substrate 11, is performed so that the cured layer 14a is removed with most of the resist pattern 14 left. According to this method, a silicon dioxide layer 16 with a high density between about 2.0 g/cm³ and about 2.1 g/cm³ and a thickness of about 20 nm or less is formed on the bottom and side faces of the interconnect grooves 15. In this case, if the anisotropic RIE process using the oxygen plasma is performed in a vacuum of 13.3 Pa or less, it is possible to form a silicon dioxide layer 16 with a high density between about 2.0 g/cm³ and about 2.1 g/cm³ and a thickness between about 10 nm and about 15 nm.

Next, the remaining part of the resist pattern 14 is removed by a wet etching process using a chemical solution that can dissolve the resist, e.g., a chemical solution containing

amine, as shown in FIG. 2E.

Subsequently, a tantalum nitride film is deposited over the second insulating film 13 as well as inside the interconnect grooves 15, or over the silicon dioxide layer 16 more exactly, by a sputtering process. Then, a copper film is deposited on the tantalum nitride film by an electroplating process. Thereafter, excessive parts of the copper and tantalum nitride films existing over the second insulating film 13, are removed by a CMP process. In this manner, metal interconnects 17 are formed inside the interconnect grooves 15 as shown in FIG. 2F. The metal interconnects 17 are made up of a barrier metal layer 17a of tantalum nitride and a main interconnect layer 17b of copper.

In the second embodiment, if the first etching method is used for the step of removing the cured layer 14a by the plasma etching process using the oxygen gas, a silicon dioxide layer 16 with a thickness of about 20 nm or less can be formed on the bottom and side faces of the interconnect grooves 15. That is to say, the thickness of the silicon dioxide layer 16 with a high dielectric constant can be reduced. As a result, a parasitic capacitance between the metal interconnects 17 can be reduced just as intended.

Also, in the second embodiment, if the second etching method is used for the step of removing the cured layer 14a by the plasma etching process with the oxygen gas, a silicon

dioxide layer 16 with a high density between about 2.0 g/cm³ and about 2.1 g/cm³ and a thickness of about 20 nm or less can be formed on the bottom and side faces of the interconnect grooves 15. In this process, if an anisotropic RIE process is performed using the oxygen plasma in a vacuum of 13.3 Pa or less, a silicon dioxide layer 16 with a high density between about 2.0 g/cm³ and about 2.1 g/cm³ and a thickness between about 10 nm and about 15 nm can be formed.

According to the second etching method, an etching process is performed in a higher vacuum (at a lower pressure) using a substrate at lower temperature and the oxygen ions has a higher energy compared to a known ashing process using oxygen plasma. Therefore, a silicon dioxide layer 16 with a high density of 2.0 g/cm³ or more can be formed. Thus, even if oxygen plasma is supplied in a subsequent process step, the oxygen ions cannot pass through the silicon dioxide layer 16, and the thickness of the silicon dioxide layer 16 does not increase. As a result, the parasitic capacitance generated between the metal interconnects 17 can be reduced just as intended.

EMBODIMENT 3

Hereinafter, a method for fabricating a semiconductor device according to a third embodiment of the present invention will be described with reference to FIGS. 3A through

FIGS. 3F.

First, as shown in FIG. 3A, a first insulating film 22 of silicon dioxide is formed on a silicon substrate 21. And a second insulating film 23 is deposited on the first insulating film 22. The second insulating film 23 is formed of a carbon-containing silicon dioxide film with a thickness of 1000 nm by a plasma CVD process or an SOG process, for example. Then, a resist pattern 24 with openings for forming interconnect grooves is defined on the second insulating film 23 as shown in FIG. 3B.

Subsequently, the second insulating film 23 is dry-etched with a plasma, thereby forming interconnect grooves 25 with a depth of about 500 nm in the second insulating film 23 as shown in FIG. 3C. Specifically, the plasma is created from an etching gas obtained by adding argon or oxygen gas to an etching gas consisting essentially of fluorine and carbon (e.g., at least one of CF_4 and CHF_3 gases). Then, the upper part of the resist pattern 24 changes into a cured layer 24a, which is made of a polymer consisting essentially of fluorine and carbon and has a thickness of about 50 nm.

Next, as shown in FIG. 3D, the cured layer 24a is removed by a plasma etching process using oxygen gas. In this process step, the resist pattern 24 under the cured layer 24a is also removed slightly, but this will not cause a serious problem. Further, a thin silicon dioxide layer 26 is formed

on the bottom and side faces of the interconnect grooves 25 in the second insulating film 23. The conditions of the plasma etching process using the oxygen gas are as described for the second embodiment, so the description thereof will be
5 omitted herein.

Thereafter, the remaining part of the resist pattern 24 is removed by a wet etching process using a chemical solution that can dissolve the resist, e.g., a chemical solution containing amine. Then, the silicon dioxide layer 26, formed on
10 the bottom and side faces of the interconnect grooves 25, is removed by a wet etching process using a chemical solution that can remove the oxide film (e.g., a chemical solution containing ammonium fluoride) as shown in FIG. 3E.

Next, a tantalum nitride film is deposited over the second
15 and insulating film 23 as well as inside the interconnect grooves 25 by a sputtering process. Then, a copper film is deposited over the tantalum nitride film by an electroplating process. Thereafter, excessive parts of the copper and tantalum nitride films, existing over the second insulating film
20 23, are removed by a CMP process, thereby forming metal interconnects 27 inside the interconnect grooves 25 as shown in FIG. 3F. The metal interconnects 27 are made up of a barrier metal layer 27a of tantalum nitride and a main interconnect layer 27b of copper.

25 According to the third embodiment, the silicon dioxide

layer 26, existing on the bottom and side faces of the interconnect grooves 25, is removed and then the metal interconnects 27 are formed inside the interconnect grooves 25. That is to say, the silicon dioxide layer 26 no longer exists between the metal interconnects 27. As a result, a parasitic capacitance produced between the metal interconnects 27 can be reduced even more significantly.

EMBODIMENT 4

10 Hereinafter, a method for fabricating a semiconductor device according to a fourth embodiment of the present invention will be described with reference to FIGS. 4A through FIGS. 4G.

First, as shown in FIG. 4A, a first insulating film 32 of silicon dioxide is formed on a silicon substrate 31. And a second insulating film 33 is deposited on the first insulating film 32. The second insulating film 33 is formed of a carbon-containing silicon dioxide film with a thickness of 1000 nm by a plasma CVD process or an SOG process, for example. Then, a resist pattern 34 with openings for forming interconnect grooves is defined on the second insulating film 33 as shown in FIG. 4B.

Subsequently, the second insulating film 33 is dry-etched with a plasma, thereby forming interconnect grooves 35 with a depth of about 500 nm in the second insulating film 33

as shown in FIG. 4C. Specifically, the plasma is created from an etching gas obtained by adding argon or oxygen gas to an etching gas consisting essentially of fluorine and carbon (e.g., gas containing at least one of CF_4 and CHF_3 gases).
5 Then, the upper part of the resist pattern 34 changes into a cured layer 34a, which is made of a polymer consisting essentially of fluorine and carbon and has a thickness of about 50 nm.

Next, as shown in FIG. 4D, a resist film 36 is deposited
10 over the entire surface of the resist pattern 34 so that the interconnect grooves 35 are filled with the film 36.

Thereafter, as shown in FIG. 4E, excessive part of the resist film 36, existing over the second insulating film 33, and the entire resist pattern 34 with the cured layer 34a in
15 its upper part are ashed away with oxygen plasma. In this process step, the plasma etching process is performed using oxygen gas for a longer time than the second embodiment by a down flow technique in a vacuum of 13.3 Pa or less. As a result, the resist film 36 and resist pattern 34 are etched
20 back. Also, after the resist pattern 34 has been removed, the upper surface (i.e., the surface other than the bottom and side faces of the interconnect grooves 35) of the second insulating film 33 of carbon-containing silicon dioxide is exposed to the oxygen plasma for just a short time. Accordingly,
25 a thin silicon dioxide layer 37 is formed in the upper part

of the second insulating film 33. On the other hand, no silicon dioxide layer is formed on the bottom and side faces of the interconnect grooves 35 because the interconnect grooves 35 are filled with the resist film 36.

5 Subsequently, as shown in FIG. 4F, the resist film 36 in the interconnect grooves 35 is removed by a wet etching process using a chemical solution that can dissolve the resist, e.g., a chemical solution containing amine.

Next, a tantalum nitride film is deposited over the second insulating film 33 as well as inside the interconnect grooves 35 by a sputtering process. Then, a copper film is deposited on the tantalum nitride film by an electroplating process. Thereafter, excessive parts of the copper and tantalum nitride films, existing over the second insulating film 33, are removed by a CMP process, thereby forming metal interconnects 38 inside the interconnect grooves 35 as shown in FIG. 4G. The metal interconnects 38 are made up of a barrier metal layer 38a of tantalum nitride and a main interconnect layer 38b of copper. In this process step, the silicon dioxide layer 37 formed in the upper part of the second insulating film 33 is also removed by increasing the thickness of the portions removed by the CMP process.

According to the fourth embodiment, in the step of removing the resist pattern 34 with the oxygen plasma, no silicon dioxide layer is formed on the bottom and side faces of

the interconnect grooves 35 because the interconnect grooves 35 are filled with the resist film 36. As a result, a parasitic capacitance, produced between the metal interconnects 38, can be reduced.

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MODIFIED EXAMPLE OF EMBODIMENT 4

Hereinafter, a method for fabricating a semiconductor device according to a modified example of the fourth embodiment will be described with reference to FIGS. 5A through
10 FIGS. 5D.

After the same process steps have been carried out as in the fourth embodiment, an ashing process is performed using oxygen plasma to remove excessive part of the resist film 36, existing over the second insulating film 33, and the entire
15 resist pattern 34 with the cured layer 34a in its upper part as shown in FIG. 5A. In this process step, the plasma etching process is performed using the oxygen gas for a longer time than the second embodiment by a down flow technique in a vacuum of 13.3 Pa or less. Then, a first thin silicon dioxide
20 layer 37 is formed in the upper part of the second insulating film 33 with no silicon dioxide layer formed on the bottom and side faces of the interconnect grooves 35 as in the fourth embodiment.

Next, as shown in FIG. 5B, the resist film 36 existing
25 in the interconnect grooves 35 is removed by a wet etching

process using a chemical solution that can dissolve the resist, e.g., a chemical solution containing amine.

Subsequently, as shown in FIG. 5C, an anisotropic RIE process, in which a bias voltage is applied to the silicon substrate 31, is performed, thereby forming a second silicon dioxide layer 39 with a high density between about 2.0 g/cm³ and about 2.1 g/cm³ and a thickness of about 20 nm or less on the bottom and side faces of the interconnect grooves 35. In this process step, if the anisotropic RIE process is performed in a vacuum of 13.3 Pa or less, it is possible to form a second silicon dioxide layer 39 with a high density between about 2.0 g/cm³ and about 2.1 g/cm³ and a thickness between about 10 nm and about 15 nm. It should be noted that the first silicon dioxide layer 37, existing in the upper part of the second insulating film 33, has its density and thickness both increased by this anisotropic RIE process. However, this will not cause a serious problem because the first silicon dioxide layer 37 will be removed by the next CMP process.

Thereafter, as shown in FIG. 5D, a tantalum nitride film is deposited by a sputtering process over the second insulating film 33 as well as inside the interconnect grooves 35 having the second silicon dioxide layer 39 formed thereon. Then, a copper film is deposited on the tantalum nitride film by an electroplating process. Thereafter, excessive parts of the copper and tantalum nitride films, existing over the sec-

ond insulating film 33, are removed by a CMP process, thereby forming metal interconnects 38 inside the interconnect grooves 35, having the second silicon dioxide layer 39 formed thereon, as shown in FIG. 5D. The metal interconnects 38 are
5 made up of a barrier metal layer 38a of tantalum nitride and a main interconnect layer 38b of copper. In this process step, the silicon first dioxide layer 37, existing in the upper part of the second insulating film 33, is also removed by increasing the thickness of the portions removed by the CMP
10 process.

According to the modified example of the fourth embodiment, it is possible to form a second silicon dioxide layer 39 with a high density between about 2.0 g/cm³ and about 2.1 g/cm³ and a thickness of about 20 nm or less on the bottom
15 and side faces of the interconnect grooves 35. Therefore, even if oxygen plasma is supplied in a subsequent process step, oxygen ions cannot pass through the second silicon dioxide layer 39. Accordingly, the thickness of the second silicon dioxide layer 39 does not increase. As a result, a
20 parasitic capacitance produced between the metal interconnects 38 can be reduced just as intended.